**Design and Pre-Layout-Simulation of the simple inverter of 65 nm**

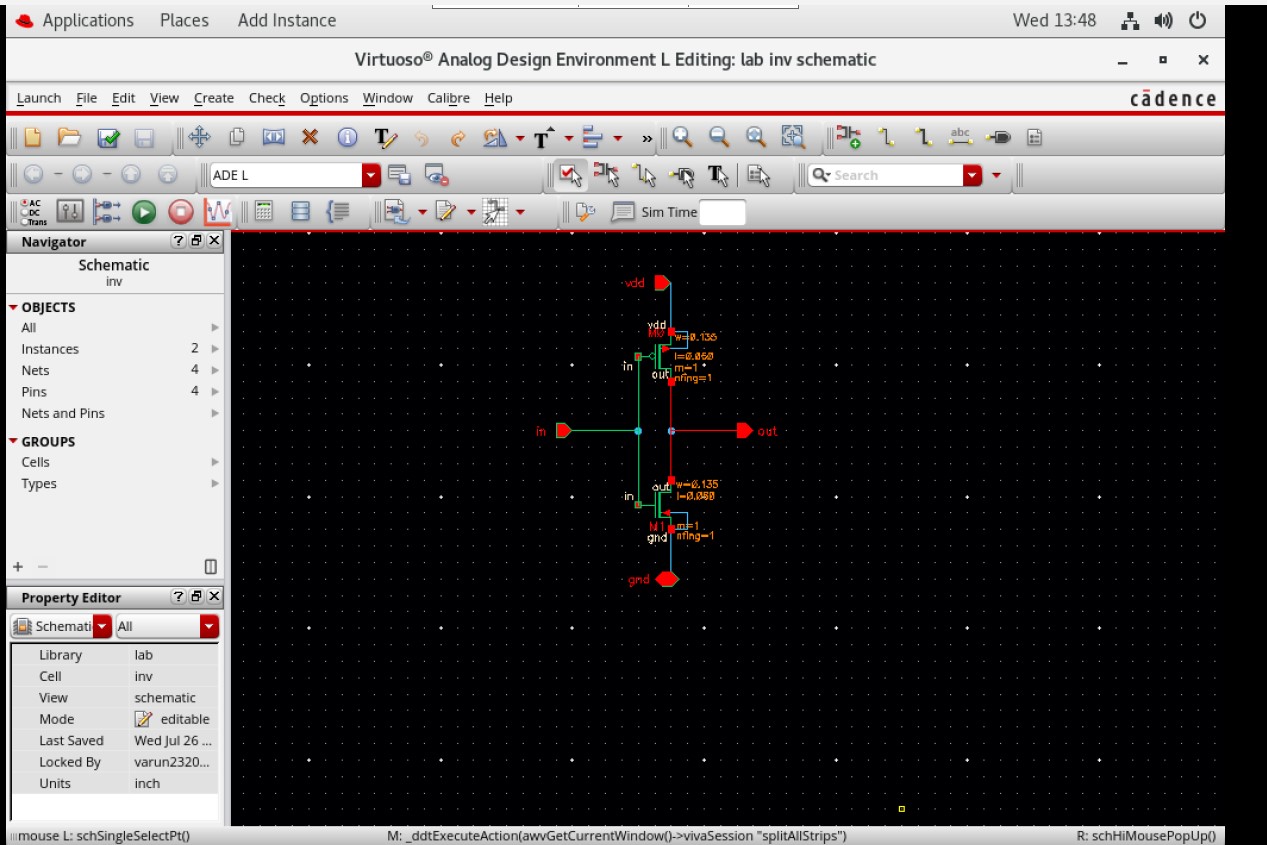
1. Make the schematic of the CMOS inverter and simulate the input-output waveform (ELDO).  
2. Calculate the delays, rise time & fall time (.meas statements).  
3. If the delays are unequal, make them approximately equal.  
4. Analyse the delays using low Vt (nlvtlp)& high Vt devices (nhvtlp) (change the model names in .src.net file).  
5. Increase the sizes of your NMOS & PMOS and analyze the effect on the delays. Provide the result on at least two dimensions.

Name-Varun Gautam

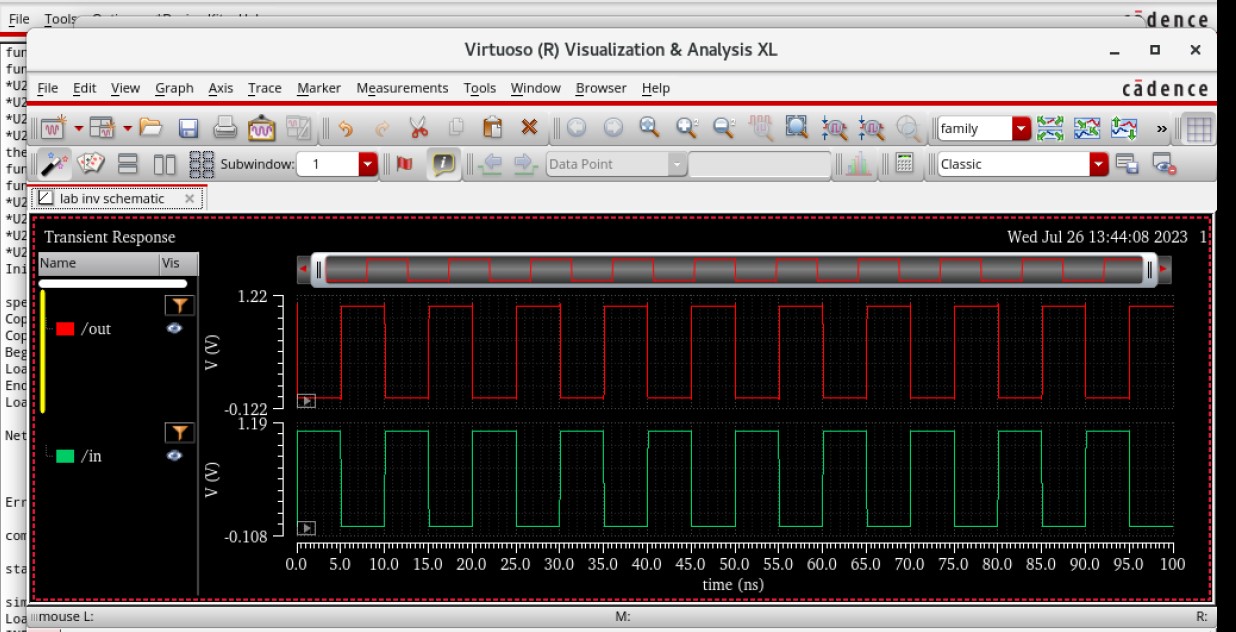
Roll no.- MT23202

Specialization-VLSI and ES

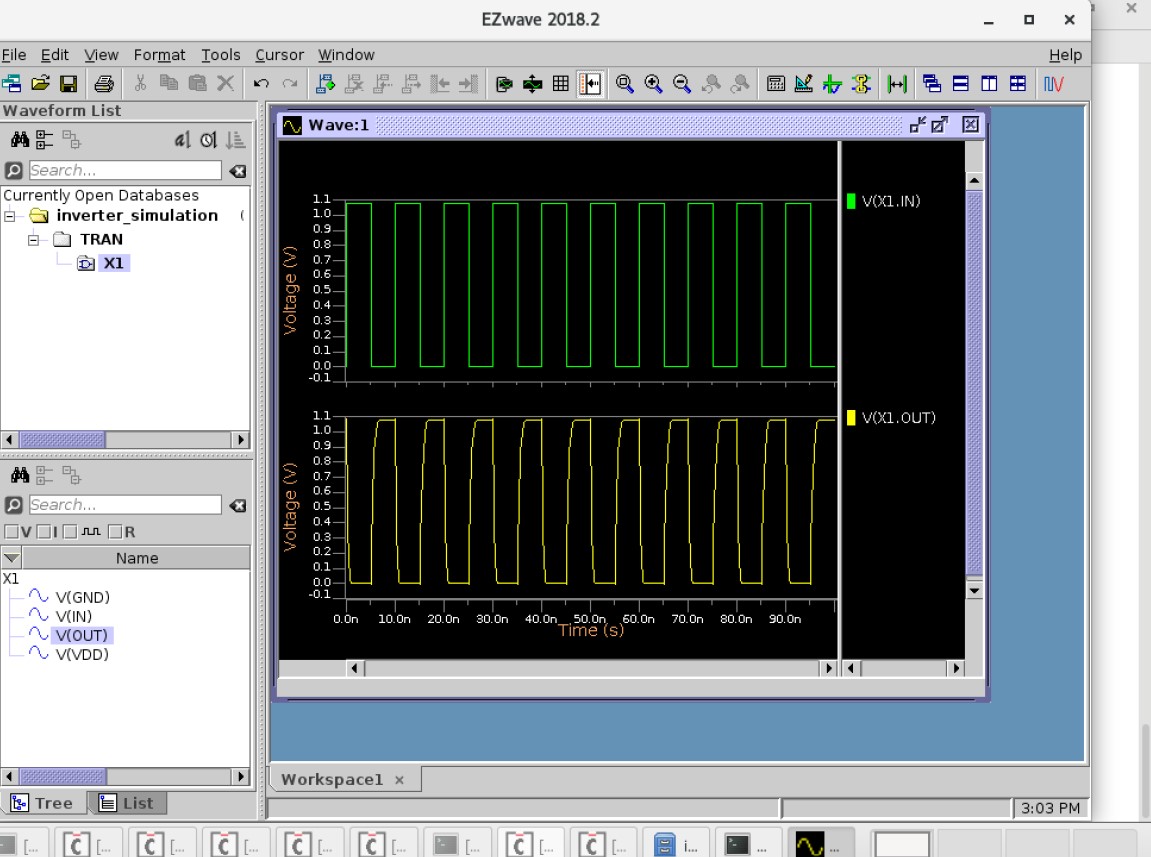
**Schematic of CMOS inverter**

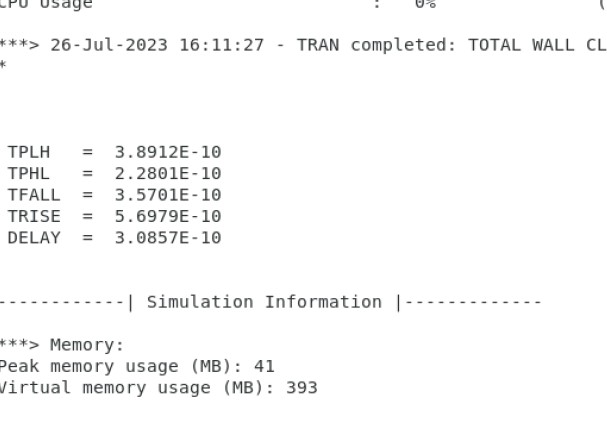


**The waveform of INPUT and OUTPUT**



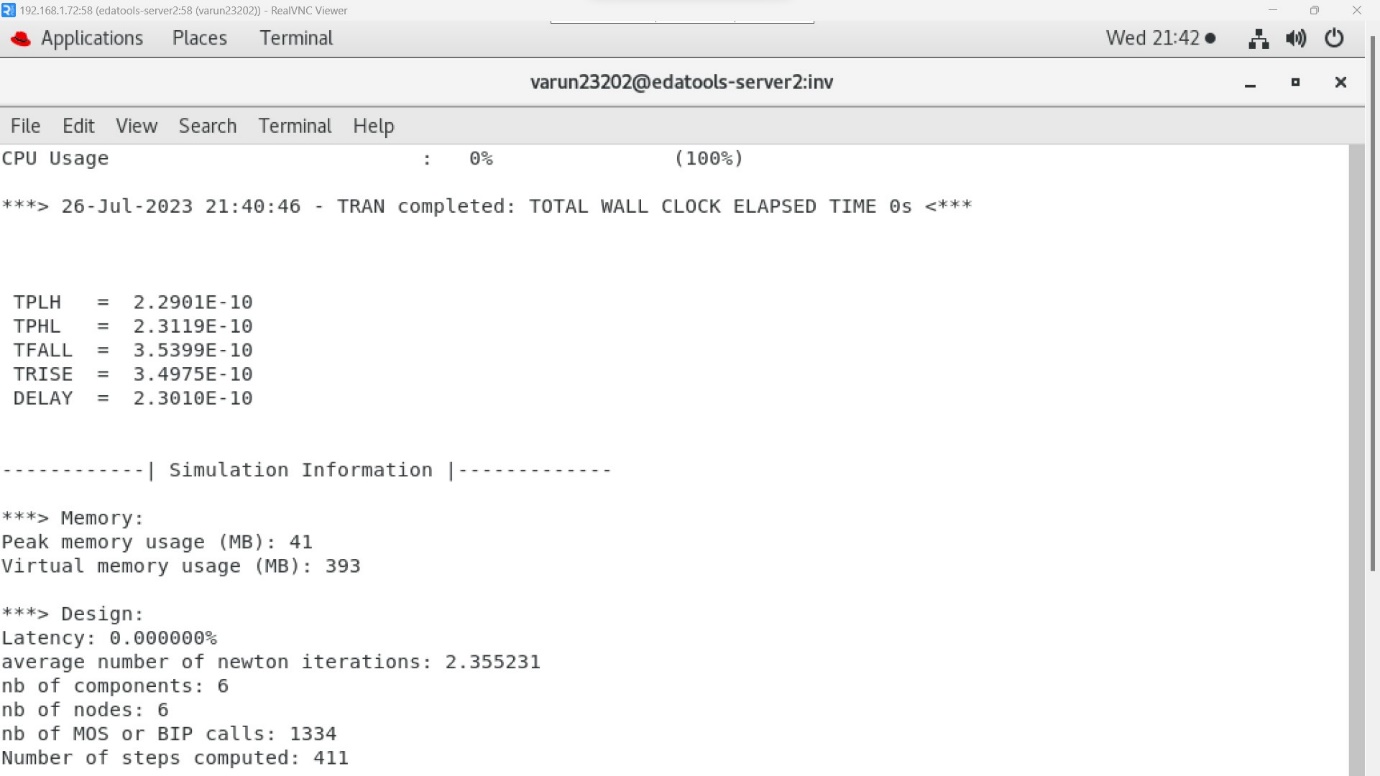
**Eldo simulation waveform**

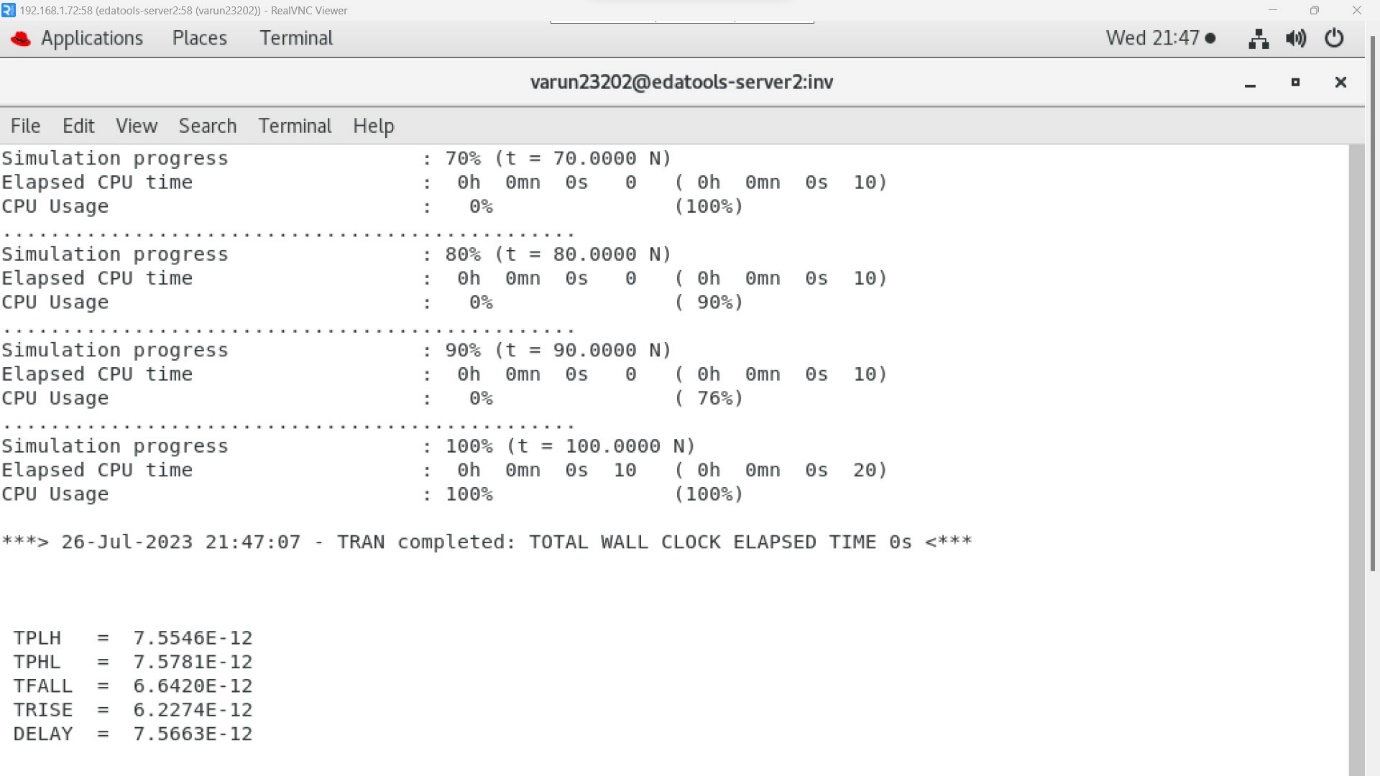


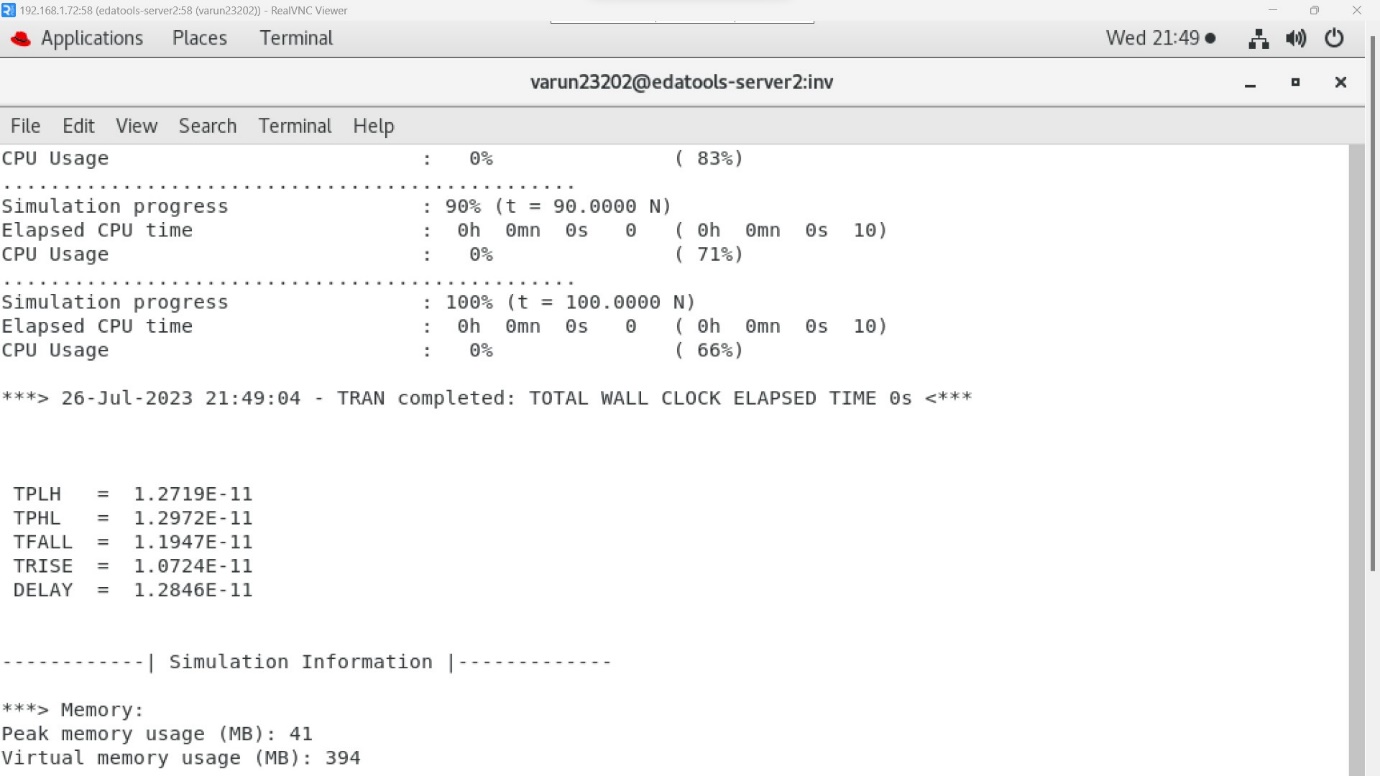
**Calculation of delays** 

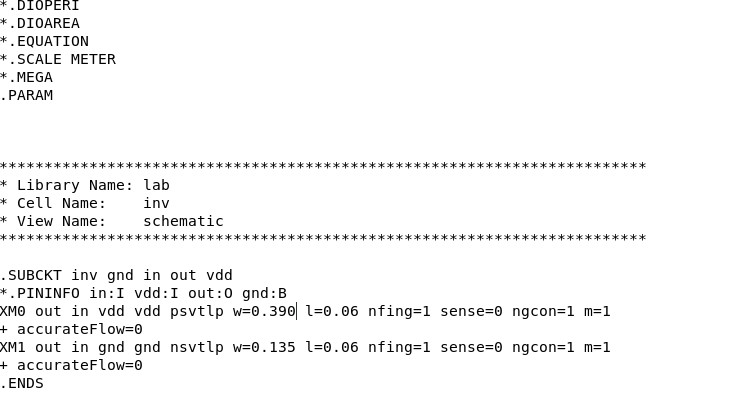
**Adjust delays by changing the width of PMOS.**

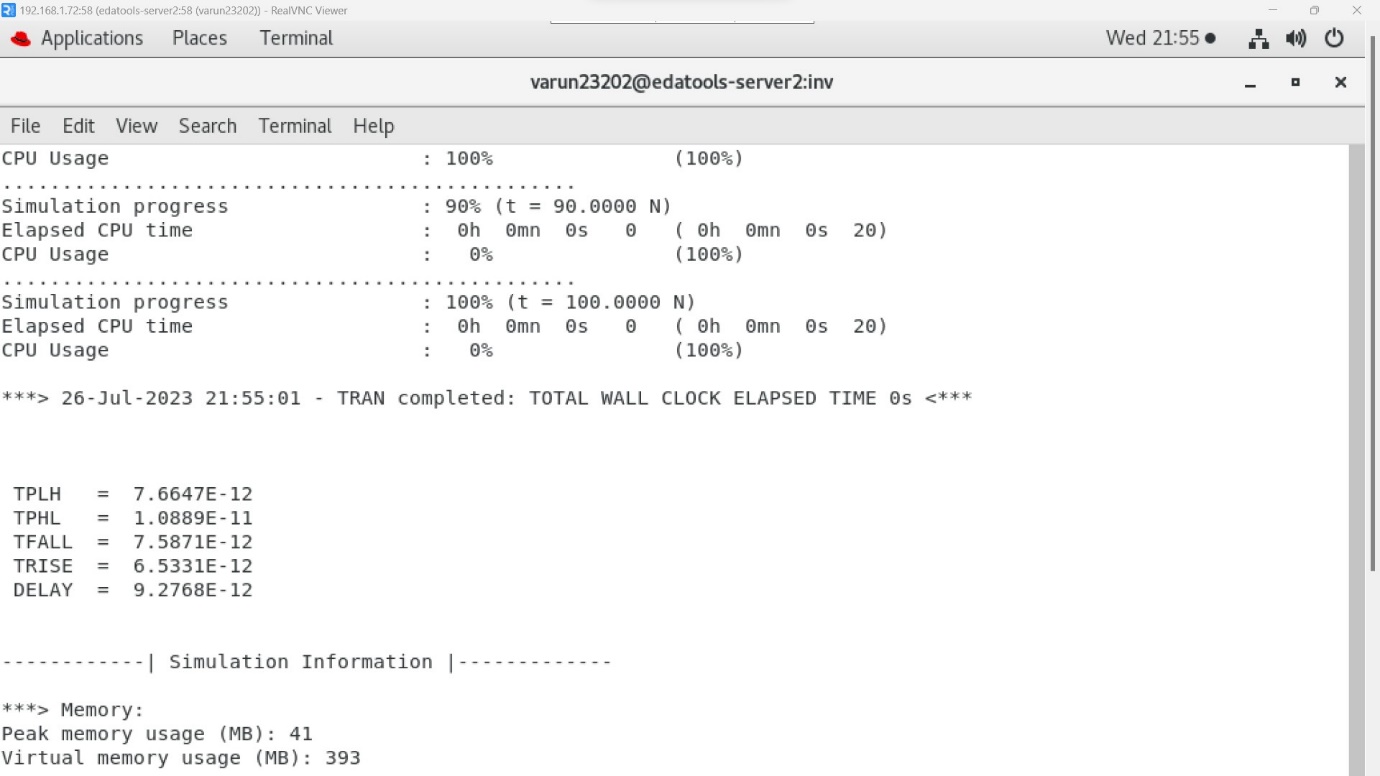
(double the width of pmos from 0.135 to 0.270)

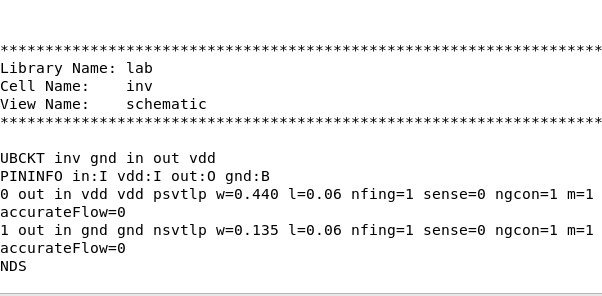


**Nlvtlp(change of model name)** 

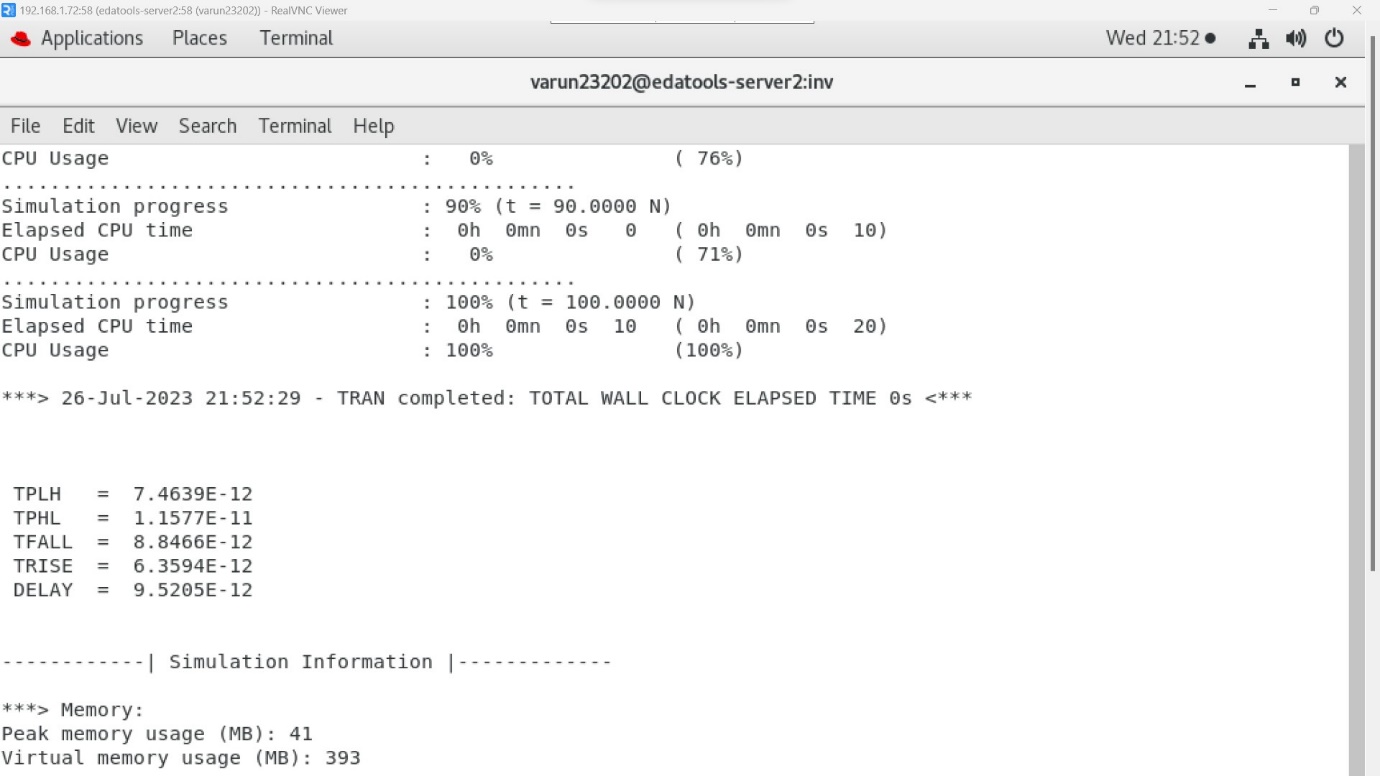
**Nhvtlp(change of model name)** 

**First size change of nmos and pmos** 

**Delays after the First size change** 

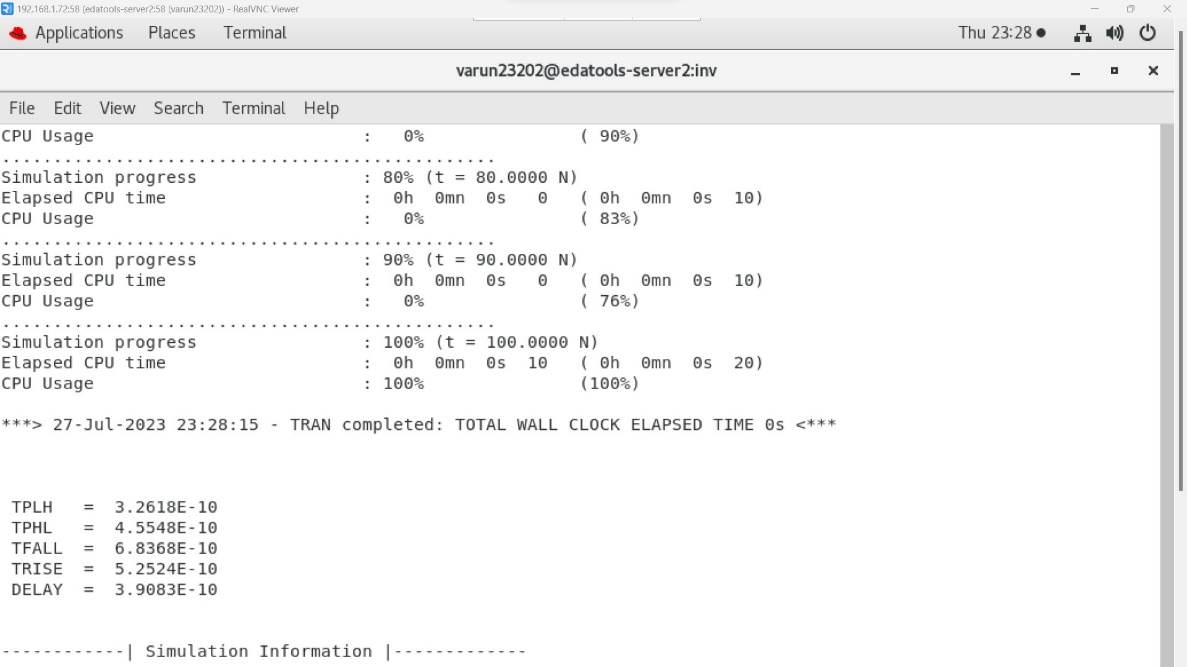
**Change of size for the second time** 

**Change of delays of Second-time size**

**change** 

**Capacitor adding**

• Change the capacitor value from 20 Farad to 40 Farad output



Analysis of